SESSIONS

JULY 18, 2018 -

Registration & Breakfast

8:00am - 9:00am

RISC-V ISA & Foundation Overview

9:00am - 9:15am

Participants

Rick O' Connor - Executive Director, RISC-V Foundation

RISCV ISA: Understanding Limitations and Methods to Improve Code Density & Performance

9:15am - 9:30am

RISC-V is an Open Architecture with Instruction Set designed for extensions from the get go. The core RISC-V Instruction Set is fairly small and it is independent of any micro-architecture or implementation style. In this study, we focused on RISC-V ISA and RISC-V Tool chain performance for ultra-low cost embedded applications. For these applications, we have chosen to investigate the RV32IMC flavor of RISC-V. The extensions were chosen with view to obtain better performance for small systems. We define the key metrics used to evaluate and assess the code density.

In this study, we have also come up with list of benchmarks and applications that we used to evaluate the architecture and tool chain. We present extensive data based on our analysis and finally make recommendations on the tool chain and ISA updates.

We will present:

- Key Performance Indicators (KPIs) for ultra-low cost embedded applications.
- Results of GNU C Compiler and LLVM C Compiler tool chain from Code Density and Performance perspective (RISCV Architecture).
- Results of GNU C Compiler tool chain from Code Density perspective for ARM Architecture. Benchmarks like coremark, dhrystone (which tend to be short) and snippets from typical Storage code (which gives deeper understanding of more real time use cases) were used for the study.
- Analysis and Recommendations for ISA extensions.
- Analysis and Recommendations for Tool Chain improvements.
- How to exploit Machine Learning techniques to study code density and performance in greater detail.

Authors:
Kalpesh Mehta – Senior Director , Flash Products Group, Western Digital
Vimal Jain – Director, Flash Products Group
Gnanasekar Rajakumar – Technologist, Western Digital
Ravikumar Gaddam – Staff Engineer, Western Digital

Participants

Gnanasekar Rajakumar - Technologist, Western Digital

Ravikumar Gaddam - Staff Engineer, Western Digital

Going Beyond the RISC-V General Purpose Solutions

9:30am - 10:00am

Processors built using the RISC-V ISA are known to be successful in the embedded/IoT domain and are heading to replace the dominance of ARM-based solutions in such applications. However, market trends show that general purpose cores will no longer survive the compute, power and performance needs of today's applications. With this in mind, InCore focuses in providing customized core/SoC solutions in the IoT sector in 3 primary domains: Security, Reliability and Intelligence. The vision is to treat security, reliability and intelligence as first-class citizens while designing RISC-V processors. This paper highlights some of the efforts undertaken by InCore in each of these verticals.

Participants

Neel Gala - CTO, InCore Semiconductors Pvt. Ltd.

Architecture Exploration of RISC-V Processor and Comparison with ARM Cortex A53 and A72

10:00am - 10:30am

This research project is focused on the architectural exploration of RISC-V ISA based processor for networking architectures such as a Router, using the trade-off between power consumption and performance. The optimized architecture is compared against commercially available RISC processors from ARM.

Participants

Karthikeyan Sugumaran - Architecture Modeling Intern, Mirabilis Design

Tom Jose - Application Specialist, Mirabilis Design

Networking Break

10:30am - 11:00am

SESSIONS

JULY 18, 2018 -

It's Not About the Core, It's About the System

11:00am - 11:30am

RISC-V is no longer just a core in the hands of academics and researchers. Consumers of these cores are now realising, that it is not just about the core, it's about the system. There is now a great deal of momentum behind RISC-V with companies building real systems of varying degrees of complexity. These systems are architected with several, sometimes even 1000s of heterogeneous processor cores -- RISC-V and others -- and many tens of other IP blocks. The software executing on such systems will be large and complex having been produced by large teams across the world. To make such systems realistic and usable, a holistic approach is needed to debug and analysis. This needs to be a system-wide approach, one which provides a coherent view of all the components within a SoC. It has to be joined up with cores, providing run-control as well as processor trace, and interconnects that non-intrusively monitor and analyze the device's internal behavior at wire speed and in the field. We present just such a debug and analytics approach, one that has been deployed in several commercial systems and one which is greatly enhancing the RISC-V ecosystem, which is extremely important for its success. Using our heterogeneous demonstration platform, we will show this in operation.

Participants

Gajinder Panesar - CTO, UltraSoC

RiTA: RISC-V Trace Analyzer

11:30am - 11:45am

Keeping in line with the vision of customizing RISC-V processors for optimum performance in specific workloads, it becomes important to obtain various statistics about program execution at the instruction level. RiTA is a simple Python tool that takes a step in this direction by analyzing the log file dumped by spike, the ISA simulator and then returning various descriptive statistics about the code. This presentation documents the basic architecture of RiTA and describes the existing and planned features.

Participants

Anmol Sahoo - Project Associate, IIT Madras

Neel Gala - CTO, InCore Semiconductors Pvt. Ltd.

Keynote: RISC-V: Enabling a New Era of Open Data-Centric Computing Architectures

11:45am - 12:10pm

Participants

Vivek Tyagi - Head Sales, Sandisk Western Digital

Networking Lunch

12:10pm - 1:30pm

Accelerating the RISC-V Revolution: Unleashing Custom Silicon with Revolutionary Design Platforms and Custom Accelerators

1:30pm - 2:00pm

Open source has revolutionized software. Now, it's hardware's turn. In this talk, I present the innovation opportunities being unleashed by making custom chips with the next generation of Freedom Platforms. I will demo our Linux-capable HiFive Unleashed board, expansion kit, and the latest AI accelerators in the ecosystem to showcase how RISC-V can be easily customized around the Freedom Unleashed Platform.

Participants

Huzefa Cutlerywala - Director, Business Development, Open Silicon | a SiFive Company

Mi-V RISC-V Embedded Ecosystem

2:00pm - 2:15pm

This presentation will showcase the growing ecosystem being built for embedded RISC-V on Microsemi's FPGA portfolio. The ecosystem includes Soft RISC-V CPUs, Design and development tools, Operating systems, Evaluation boards, and solutions such as Linux PC and Deep Learning implemented on our Mi-V Unleashed expansion board and the SiFive Unleashed board. Also introducing X-WARE IoT Platform solution from expresslogic.

Participants

Krishnakumar Ranamoorthi - Sr. Staff Product Marketing, Microsemi

Verification of the PULPino SoC platform using UVM

2:15pm - 2:30pm

As RISC-V gains popularity and its use in semiconductor devices grows, it becomes increasingly important to start looking at verification of these SoCs based on RISC-V. An SoC is typically characterized by the processor (RISC-V) and an associated set of peripheral devices on chip. It is not uncommon to find an SoC having communication links to external world through interfaces such as USB, SPI, i2C etc. Verification of these SoCs offer several challenges, the chief among them being the hardware-software interface between the software test code running on the CPU and the hardware external peripherals such as SPI slave. Although several verification techniques exist the Universal Verification Methodology is currently becoming the standard among all semiconductor companies. In this project we have verified the RTL of the PULPino platform using UVM.

Participants

Mahesh R - Associate Engineer, Cisma Consultants Pvt Ltd

Shamanth HK - Associate Verification Engineer, Cisma Consultants

SESSIONS

JULY 18, 2018 -

Porting Graphical Stacks to RISC-V using QEMU and Yocto

2:30pm - 2:45pm

For RISC-V to compete with other incumbent architectures outside of the very small single-use embedded space it will need support to run a Graphical User Interface (GUI). Even in embedded devices users are accustomed to easy to use GUIs such as that presented by Android and iOS. With the rise of open source software and people becoming increasingly privacy conscious, there is a growing number of open source smartphone software stacks that compete against Android and iOS. Plasma Mobile is one example of a complete software system for mobile devices with a strong focus on users' privacy protection. It has an active development community behind it, backed by the KDE desktop environment project developers and is running on real ARM hardware today.

This presentation explores the process of building Plasma Mobile for RISC-V using Yocto. Yocto is a Linux Foundation backed project whose goal is to allow the creation of Linux distributions specifically for embedded devices. This requires cross compiling the entire dependency chain from QT5 and Xorg to Plasma.

We also discuss testing of this mobile environment using the RISC-V model in QEMU, including a PCIe attached GPU. This allows easy development and testing without RISC-V hardware. QEMU has a much quicker turnaround time than real hardware allowing faster development cycles. As an additional advantage QEMU has been setup to model the RISC-V hardware, allowing a quick and easy transition to running the software stack on hardware when a GPU becomes available.

This presentation will walk through the changes required to Yocto and the corresponding software projects to cross compile the full Plasma Mobile stack to for RISC-V and get a graphics stack up and running. It will also detail additional work done to ensure that the required kernel drivers are enabled and that the correct configuration is used.We will also discuss the changes to QEMU to allow this testing, along with current limitations and what can be done in the future to improve the RISC-V ecosystem.

Participants

Atish Patra - Principal R&D Engineer, Western Digital

Networking Break

2:45pm - 3:15pm

Panel: Evolving a RISC-V based Ecosystyem in India

3:15pm - 4:15pm

Participants

Panelist: Vivek Tyagi - Head Sales, Sandisk Western Digital

Panelist: Konala Varma - Business Head - Smart Devices, Intel

Panelist: Mahesha Nanjundaiah - Director, HPE Research, HPE

Panelist: Asutosh Upadhyay - Head - Programs, Axilor Ventures

Panelist: Amudhan Balasubramanian - General Manager, HCL Technologies

Moderator: G S Madhusudan - CEO and Co-Founder, InCore Semiconductors

Poster / Demo Previews

4:15pm - 5:00pm

- Variable Precision RISC-V Co-processor for Scientific Applications, Andrea Bocco & Tiego Trevian Jost, CEA LETI
- RVS - A Verification Suite to Test Compliance with RISC-V Architecture, Shubhodeep Roy Choudhury
- RISC-V open-source models and virtual platforms coupled with commercial grade simulation technologies and tools, Kevin McDermott, Imperas
- Multi-level Interrupt Design in RISC-V Linux, Atish Patra, Western Digital

Participants

Andrea Bocco - PhD Candidate, CEA-Leti

Shubhodeep Choudhury - CEO, Valtrix

Tiago Jost - Ph.D. Candidate, ENS Paris and CEA

Kevin McDermott - CTO, Imperas Software

Atish Patra - Principal R&D Engineer, Western Digital

Evening Reception, Poster Sessions and Demos

5:00pm - 8:00pm

SCHEDULE

JULY 18, 2018 -

RISC-V Workshop Chennai

18 - 19 July 2018
Indian Institute of Technology Madras
Chennai

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8:00AM	**8:00am** - Registration & Breakfast
9:00AM	**9:00am** - RISC-V ISA & Foundation Overview **9:15am** - RISCV ISA: Understanding Limitations and Methods to Improve Code Density & Performance **9:30am** - Going Beyond the RISC-V General Purpose Solutions
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12:00PM	**12:10pm** - Networking Lunch
1:00PM	**1:30pm** - Accelerating the RISC-V Revolution: Unleashing Custom Silicon with Revolutionary Design Platforms and Custom Accelerators
2:00PM	**2:00pm** - Mi-V RISC-V Embedded Ecosystem **2:15pm** - Verification of the PULPino SoC platform using UVM **2:30pm** - Porting Graphical Stacks to RISC-V using QEMU and Yocto **2:45pm** - Networking Break
3:00PM	**3:15pm** - Panel: Evolving a RISC-V based Ecosystyem in India
4:00PM	**4:15pm** - Poster / Demo Previews
5:00PM	**5:00pm** - Evening Reception, Poster Sessions and Demos

SESSIONS

JULY 19, 2018 -

Registration & Breakfast

8:00am - 9:00am

RISC-V Software Development Methodology for RISC-V Devices with RTOS and Linux or Both

9:00am - 9:30am

As RISC-V based devices start to appear in the market many software development project will start to focus on the details around porting of various OS and RTOS plus the associated work on driver development and bring up of legacy software. The key to the success of RISC-V will be the support and tools needed to drive broad adoption throughout the embedded software developer community. The embedded systems community is increasingly complementing hardware-based software development with virtual prototypes to achieve higher software quality and reduce software engineering schedules. Virtual platforms, offer advantages over hardware based development platforms in controllability, observability, repeatability, and ease of automation. Plus virtual platforms can also be available to the entire software team months before hardware platforms can be used, so provide an early start for software tasks. At a higher level than the actual development platforms, embedded software teams are also using Agile methodologies, including Continuous Integration (CI). This modern methodology for embedded software development, debug and test will be discussed and the complementary nature of virtual and hardware platforms will be shown. Including the bring up of FreeRTOS on a RV32I platform and also Linux with an example application utilizing custom instructions.

Participants

Kevin McDermott - CTO, Imperas Software

Linux Kernel on RISC-V: Where do we stand?

9:30am - 10:00am

The momentum behind RISC-V ecosystem is really commendable and its open nature has a large role in its growth. It allowed contributions from both academic and industry community leading to an unprecedented number of hardware designs proposals in a very short span of time. However, RISC-V software ecosystem also need to grow across the stack so that RISC-V can be a true alternative to existing ISA. Linux kernel support holds the key in this. This talk will serve two goals. First, it will summarize the current capabilities of Linux on RISC-V to guide application developers toward appropriate design choices for early prototyping and performance benchmarking. And second, the presentation will help to guide new developers willing to start contributing towards the RISC-V kernel port and its ecosystem by pointing out areas of the support lacking or in need of more work. As a conclusion to this presentation, we will also share our RISC-V experience, the difficulties encountered and how they were resolved to help other developers a faster transition to this exciting new architecture.

Participants

Atish Patra - Principal R&D Engineer, Western Digital

A Comprehensive Framework For Power-based Side-channel Leakage Evaluation of SHAKTI C-Class

10:00am - 10:30am

This work proposes a framework for evaluating data-leaks on SHAKTI C-Class (a RISC-V based microprocessor) through power-consumption side-channels. The work provides a comprehensive analysis of various metrics and techniques that have been proposed in literature to analyse data leaks due to such side-channels. The evaluation is done using a novel framework based on a Hamming Distance metric for modelling power patterns on binary data. The work further explores the cause of such data leaks and identifies architectural designs and practices which lead to such data leakages in the context of SHAKTI C-Class processor.

Participants

Muhammad Arsath - Student, IIT Madras

Chester Rebeiro - Assistant Professor, Indian Institute of Technology Madras

Networking Break

10:30am - 11:00am

RISECREEK: From RISC-V Spec to 22FFL Silicon

11:00am - 11:30am

SHAKTI is a series of micro-processor SoCs which target various applications ranging from small micro-controllers to server class applications. This paper describes the first Shakti SoC, code-named "Risecreek", that has been taped out on Intel's 22nm technology node. Risecreek is a test SoC designed around the open-sourced Shakti-C64 which is a 64-bit, 6-stage in-order pipelined microprocessor. It implements the RISCV-ISA and supports RV64IMAFD in- struction set (user specification v2.2). The microprocessor has a Memory Management Unit that supports sv39 vital- ization scheme and is compliant with the RISC-V privilege specification v1.10. The microprocessor includes a bimodal Branch Predictor Unit (BPU) with a Return Address Stack (RAS), 32KB Virtually Indexed Physically Tagged (VIPT) I-cache and D-cache, multi-cycle Single Precision (SP) and Double Precision (DP) Floating Point Units (FPU), and an AXI4-bus fabric for the peripherals. The various peripher- als that are integrated on the Risecreek SoC include I2Cs, QSPIs, UARTs, Timer, Platform Level Interrupt Controller (PLIC), JTAG controller, SDRAM controller, multi-channel DMA and also a custom expansion peripheral to connect to an FPGA. The complete SoC was designed using Bluespec System Verilog (BSV) and includes no 3rd party IPs. All pe-ripherals, controllers, engines are home-grown/ modified and open source on the SHAKTI bitbucket repository.

Participants

Vinod Ganesan - Student, IIT Madras

Gopinathan Muthuswamy - Project Associate, IIT Madras

Shakti M-Class Libre RISC-V SoC

11:30am - 12:00pm

Most commercial mass-volume processors are designed based on reducing each of hard macro licensing cost, royalties, and risk. Proprietary hard macros are chosen based on the fact that they are tried-and-tested. Unfortunately the software libraries they come with are often also proprietary, particularly in the 3D and Video space. The Shakti Group however has an over-riding requirement that the entire hardware design files and associated software drivers must be entirely libre-licensed, so that it may be independently audited, to ensure no spying back-doors in the hardware, or trojans built-in to the proprietary software. This paper therefore outlines a plan on how to design and bring to market a mass-volume commercial System-on-a-Chip that prioritises BSD-licensed hard macros at the top of the list.

Participants

Luke Leighton - Software Libre Engineer and Advocate, Independent

SESSIONS

JULY 19, 2018 -

SLSV : The Shakti LockStep Verification Framework

12:00pm - 12:30pm

The Shakti LockStep Verification (SLSV) Framework is a Dynamic Verification and post-silicon Validation Framework for RISC-V System on Chip solutions. SLSV allows designers to perform functional verification with directed and random test vectors against target device(s) under verification (DUV) right from RTL to Silicon. SLSV tracks relevant architectural and micro-architectural states and evaluates them against a specified golden model. The golden model can be a functional simulator/emulator or a synthesizable formal model. SLSV can presently operate with any RISC-V design with an SLSV compatible interface and currently supports designs compliant to the debug spec 0.13. The benefit of SLSV lies in the customizability of the coverage metrics & model checkers being observed by the user. SLSV provides a configurable script-like interface enabling the user to configure and track different micro-architectural states. SLSV further empowers quick fault localization and thereby speed-up RISC-V compliance. SLSV is a completely open-source framework being developed at IIT-Madras and can be found at : github.com/command-paul/slsv-master

Participants

Paul George - Student, Shiv Nadar University

Lavanya Jagan - Project Associate, IIT Madras

Networking Lunch

12:30pm - 2:00pm

A Survey of E31 RISC-V Core Floor-Plan and Its Impact on Power, Performance and Area (PPA)

2:00pm - 2:30pm

E31, a RISC-V core from SiFive Inc., has an instance count of about 112k post synthesis, excluding memories. Due to huge instance count, the turn-around time for any PNR tool will be large, leading to delays in final SoC tape-out. In this paper, we did a survey of modularizing E31 core, pre-placing these new mid-size modules with fixed pin locations and leveraging hierarchical PNR feature of an EDA tool. Results shows, this approach reduces the turn-around time by more than 80%, while ensuring a similar/better PPA of entire core compared to flat PNR approach. This paper uses all open-source EDA toolset from opencircuitdesign.com, and 0.18um technology node from OSU standard cell library.

Participants

Kunal Ghosh - Director, VLSI System Design Corporation Pvt. Ltd.

Anagha Ghosh - Director, VLSI System Design Corporation Pvt. Ltd.

Integrating Gen-Z in Server-Class RISC-V Processors

2:30pm - 3:00pm

Gen-Z is a new open systems Interconnect created to provide memory semantic access to data and devices via direct-attached, switched for fabric topologies, and will accelerate the adoption of rack level composability. This talk will cover an overview of Gen-Z, and focus on implications for processors. A native implementation of Gen-Z will place requirements on the processor architecture, and we will explore some of these areas like number of lanes to be supported, memory mapping using ZMMUs, Gen-Z atomics and security features like page level encryption.

Participants

Mohan Pathasarathy - Technical Architect, HPE

Formal Specification of the RISC-V Instruction Set Architecture

3:00pm - 3:30pm

The ISA Formal Specification Task Group was created by the RISC-V Foundation. In this talk, we describe what is a formal spec, its purpose, and how it will be used by verifiers, compiler writers and hardware designers, not only as an unambiguous and precise reference, but also to formally prove correctness of the artifacts they are designing. We describe the subtleties induced by requiring ``universality'' (model all possible RISC-V implementations), modularity (many RISC-V features are optional extensions), and concurrency (non-determinism due to the Weak Memory Model interacting with optimizations such as pipelining, speculation, and cacheing).

The Task Group is pursuing several approaches; we will show excerpts, describe how to use it as an executable 'golden reference model', and describe how it is already being used by some groups in design and verification.

Participants

Rishiyur Nikhil - Chief Technology Officer, Bluespec

Niraj Sharma - Head, India, Bluespec

RISC-V Workshop Chennai Conclusion

3:30pm - 3:45pm

Participants

Rick O' Connor - Executive Director, RISC-V Foundation

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3:00PM	**3:00pm** - Formal Specification of the RISC-V Instruction Set Architecture **3:30pm** - RISC-V Workshop Chennai Conclusion