SESSIONS

PRECONFERENCE, DECEMBER 3, 2018 - 03/12/2018

Registration: Open 9AM - 6PM

9:00am - 10:00am

Tutorial: Running the Zephyr RTOS and Machine Learning with TensorFlow Lite on RISC-V

10:30am - 12:00pm
Track 1

Edge AI capabilities of modern systems enable machine learning tasks to be performed closer to where the data is being produced, eliminating the need for power-inefficient communication with the cloud, minimizing privacy concerns and reducing latency. Originally targeting smartphones, Google's TensorFlow Lite framework now ventures to support even very small devices in performing ML tasks in a unified and user-friendly way, and has recently added RISC-V support. The Zephyr RTOS on the other hand enables a Linux-like programming experience for small embedded devices, providing a unified OS platform for use cases where Linux is simply too big.

In this tutorial, we will show how RISC-V can be used on edge devices to run a standard RTOS and perform machine learning tasks on RISC-V hardware. You will learn about current status of Zephyr and TF Lite and plans for TF Lite RISC-V support, developing with Zephyr and TF Lite on real hardware, testing with the open source Renode framework, and more.

Location: 2nd Floor Meeting Rooms 209/210

Participants

Pete Warden - Staff Research Engineer, Google

Peter Zierhoffer - Team Leader -- Renode, Antmicro

Lunch

12:00pm - 1:30pm
Track 1

Lunch

12:00pm - 1:30pm
Track 2

Formal Verification of RISC-V processor implementations -- Space Limited!

1:30pm - 3:00pm
Track 1

Location: 2nd Floor Meeting Rooms 209/210

Learn how to use formal Assertion Based Verification (ABV) and open-source tools to formally verify HDL designs, and how to use the properties and formal test benches in the riscv-formal framework to formally verify RISC-V cores with ease.

This tutorial is aimed specifically at HDL design engineers without in-depth knowledge of formal methods who want to add formal ABV to their verification toolbox.

Participants

Edmund Humbenberger - CEO, Symbiotic

Clifford Wolf - CTO, Symbiotic EDA

Running a Linux-Capable Open Source Soft SoC on the Avalanche Board with MicroSemi PolarFire FPGA

1:30pm - 3:00pm
Track 2

Location: 2nd Floor Meeting Rooms 203/204

As an open and flexible standard, the RISC-V ISA is an excellent match for both ASIC and FPGA implementations. The availability of open source cores with mainstream tooling is breathing new life into the open hardware and IP space, making it feasible for the first time to create open source SoCs which can be made available to everyone at no cost other than a simple board. With open tooling support and a connection to the broader RISC-V ecosystem, the open source soft FPGA SoC based on LiteX/VexRiscV can serve as an entry point to open source digital design. The open source SoC running Linux on the new MicroSemi PolarFire FPGA will be presented and explained, and the capabilities offered by a flexible, Linux-enabled FPGA RISC-V platform will be discussed and explored in this tutorial by Antmicro and Microchip.

Participants

Karol Gugala - Team Lead, Antmicro

Bill Pratt - Regional Technical Director, Future Electronics

Networking Break

3:00pm - 3:30pm
Track 1

Networking Break

3:00pm - 3:30pm
Track 2

Tutorial: Easy-to-use, FPGA-Accelerated Hardware Simulation of RISC-V Hardware Designs with FireSim on Amazon EC2 F1

3:30pm - 5:00pm
Track 2

Location: 2nd Floor Meeting Rooms 203/204

We present a tutorial for FireSim (https://fires.im), an easy-to-use, open-source, FPGA-accelerated cycle-accurate hardware simulation platform developed at UC Berkeley that runs on Amazon EC2 F1. FireSim automatically transforms and instruments open-hardware designs (e.g. RISC-V Rocket Chip and BOOM) using the MIDAS framework into fast, deterministic, FPGA-based simulators that enable productive pre-silicon verification and performance validation. By providing a framework to automate the management of FPGA infrastructure, FireSim also lets software developers get a head-start on building software for a novel hardware design, by letting these developers interact with the pre-silicon hardware design as they would a virtual machine. In effect, both hardware and software developers work from a single source of truth: the RTL for the hardware design. Leveraging AWS EC2 F1, FireSim removes the high capex and management complexity traditionally involved in large-scale FPGA-based simulation, democratizing access to realistic pre-silicon hardware modeling of new designs. In this half-day tutorial, we cover the open-source FireSim framework, explore how users can use and modify the existing designs available in FireSim, and show how users can integrate and measure their own hardware designs.

Participants

Alon Amid - Graduate Student, UC Berkeley

Sagar Karandikar - Graduate Student, UC Berkeley

David Biancolin - Graduate Student, UC Berkeley

RISC-V Summit Welcome Happy Hour -- Sponsored by Ashling

5:00pm - 7:00pm

Join us at the "Welcome to the RISC-V Summit" Happy Hour, celebrating the first RISC-V Summit! Doors open on Dec. 3rd at 5pm. Don't miss your chance to network over drinks with your peers, colleagues and industry luminaries.

Location: 2nd Floor Meeting Rooms 209/210

SCHEDULE

PRECONFERENCE, DECEMBER 3, 2018 - 03/12/2018

TIME	TRACK 1	TRACK 2
9:00AM	**9:00am** - Registration: Open 9AM - 6PM	**9:00am** - Registration: Open 9AM - 6PM
10:00AM	**10:30am** - Tutorial: Running the Zephyr RTOS and Machine Learning with TensorFlow Lite on RISC-V	
11:00AM		
12:00PM	**12:00pm** - Lunch	**12:00pm** - Lunch
1:00PM	**1:30pm** - Formal Verification of RISC-V processor implementations -- Space Limited!	**1:30pm** - Running a Linux-Capable Open Source Soft SoC on the Avalanche Board with MicroSemi PolarFire FPGA
2:00PM		
3:00PM	**3:00pm** - Networking Break	**3:00pm** - Networking Break **3:30pm** - Tutorial: Easy-to-use, FPGA-Accelerated Hardware Simulation of RISC-V Hardware Designs with FireSim on Amazon EC2 F1
4:00PM		
5:00PM	**5:00pm** - RISC-V Summit Welcome Happy Hour -- Sponsored by Ashling	**5:00pm** - RISC-V Summit Welcome Happy Hour -- Sponsored by Ashling

SESSIONS

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

Registration Open: 7:30 AM - 6:30 PM

8:00am - 8:20am
Keynotes

Welcome & RISC-V ISA & Foundation Overview

8:20am - 8:40am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Rick O' Connor - Executive Director, RISC-V Foundation

RISC-V State of the Union

8:40am - 9:10am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Krste Asanovic - Professor / Chief Architect, UC Berkeley | SiFive

Unleashing Innovation from Core to Edge

9:10am - 9:40am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Big Data and Fast Data applications are transforming enterprise environments involving core activities on-premises and on hyper-scale cloud infrastructure, as well as those that occur at the network's edge, with new hubs or "data depots" emerging to address the locality and speed of access to data. Regional, local and remote data centers, and/or points of data aggregation, now provide opportunities to transform and add value to data as it flows from IoT and other edge applications, into the core of the network where it can be processed and analyzed to deliver actionable insights and value. Each of these data depots will require unique compute architectures and advanced data processing requirements paving the way for RISC-V -- an open instruction set architecture (ISA) designed to meet the diverse application needs of Big Data and Fast Data in this data-centric world. In this keynote, Western Digital CTO Martin Fink will discuss the value of purpose-built compute architectures and how RISC-V will enable a diversity of Big Data and Fast Data applications and workloads at each point along the spectrum, from edge to core.

Participants

Martin Fink - Executive Vice President and Chief Technology Officer, Western Digital

Enabling the Freedom to Innovate

9:40am - 10:00am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Patrick Johnson - Vice President, Mixed Signal and FPGA Business Units, Microchip

Networking Break

10:00am - 11:00am
Keynotes

Exhibit Hall Open: 10AM - 7PM

10:00am - 10:50am
Expo

Location: 1st Floor, Exhibit Hall A-2 & A-3

RISC-V Linux Hackathon: 10AM - 7PM

10:50am - 11:40am
Expo

Don't miss out on the RISC-V Linux Hackathon, happening Dec. 4-5 on the Expo Floor at the RISC-V Summit.

Watch as a team of 10 expert hackers create cutting edge applications on a soft RISC-V CPU running Linux on the low-cost Avalanche FPGA board.

The 100X Problem – How to Redefine Silicon for Augmented Reality

11:00am - 11:30am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Robert Shearer - Director of Silicon Architecture and Modeling, Facebook

Lunch & Exhibit Hall Visit

11:40am - 1:10pm
Main Agenda

Expo Hall Open 10:00 AM - 7:00 PM

11:40am - 12:25pm
Expo

Location: 1st Floor, Exhibit Hall A-2 & A-3

Birds of Feather Discussion: Debugging + Tracing

12:00pm - 12:45pm
Birds of a Feather

Location: 2nd Floor Meeting Rooms 203/204

Implementing an effective debugging system is crucial for efficient software development, and supporting a new bare metal multicore system in a debugger requires careful design and implementation choices. These choices depend on the programming and memory models of the target system -- there is no one-size-fits-all solution. In this discussion session, we outline the options and how they map onto targets with different characteristics. The GNU Debugger (GDB) and the Open On-Chip Debugger (OpenOCD) support RISC-V targets, but requires customization for each new multicore target. It is relatively straightforward to decide if, and which of, the single-inferior options are appropriate. For multi-inferior, if the target has in practice either a fully-shared or fully-disjoint address space for each core, then the single- or multiple-address space options are appropriate. Most implementations have a mix of the two. We implemented GDB and a GDBServer for a 36-core RISC-V system. For this scenario, multiple inferiors was an appropriate choice. On top of this, we implement hosted IO for each core. By freeing-up hardware engineers from learning "how to" hack on GDB absorbing precious engineering time it increases output from hardware engineers whilst delivering optimal product outcomes.

Participants

Graham Markall - Senior Compiler Engineer, Embecosm

RISC-V Linux Hackathon: 10AM - 7PM

12:25pm - 1:10pm
Expo

Don't miss out on the RISC-V Linux Hackathon, happening Dec. 4-5 on the Expo Floor at the RISC-V Summit.

Watch as a team of 10 expert hackers create cutting edge applications on a soft RISC-V CPU running Linux on the low-cost Avalanche FPGA board. Thanks to Western Digital for organizing!

SESSIONS

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

CPU Project in Western Digital: From Embedded Cores for Flash Controllers to Vision of Datacenter Processors with Open Interfaces

1:10pm - 1:30pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Rooms 203/204

RISC-V Instruction Set Architecture has become a key driver for driving open source projects across wide gamut of end applications. Most recently we have seen a lot of application in the Internet of Things (IoT) segment, microcontrollers for a variety of traditional embedded applications, and applications requiring capability for low power operation of inference engines based on artificial neural networks.

In Western Digital, we have developed super-scalar (2-way) 9-stage pipeline mostly in-order, open-source core ECHX1, targeting in-house embedded Storage System on Chip (applications). In this paper, we plan to present some of the architectural details of the core, and challenges in the implementations, as well as discuss application of the core for the Flash controller. Additionally, we will explain the vision for expansion of RISC-V cores into datacenter and enterprise market.

We believe that open interface architectures will be key drivers of datacenter applications in 2023. We are witnessing computation shifting to dedicated machine learning and inference accelerators (also based on RISC-V Cores!) , and fast data migrating to large low latency, persistent memory pools. In this new world, the main processor interface connectivity capabilities, in particular bandwidth, latency and cache coherence capability for efficient memory sharing are becoming more relevant than raw compute capability of the cores.

We will discuss open interfaces for persistent memories, such as JEDEC-standardized NVDIMM-P (Non-volatile dual inline memory module for persistent memories), and also exporting cache-coherence protocols (such as Tilelink) over ubiquitous fabrics such as Ethernet. We plan to discuss details of the MPF4brik â€“ memory protocol fabrik, which exposes Tilelink on the Ethernet, and allows smart switching using P4-based programmable networking. We are envisioning low-cost SMP (symmetric multiprocessing) architectures based on open standards, which will enable hyperconvergence of processing and memory in the future datacenter.

Participants

Zvonimir Bandic - Program Co-Chair, RISC-V Summit | Sr. Director, Next Gen Platform Technologies, Western Digital

Dejan Vucinic - Director, NVM Systems Architecture, Western Digital

Robert Golla - Senior Fellow, Western Digital

Deterministic L2 Cache Solution and Performance in an AMP capable SoC

1:10pm - 1:30pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

Linux based embedded systems may need to execute real-time tasks from time to time. A Linux based motor control solution is a good example of such a system. While Linux may offer a rich execution environment, it is not practical to control motors in real time. This presentation will compare and contrast various solutions to this problem such as Overwhelming the Linux system with bandwidth, Adding a real-time controller to the system, and Provisioning an AMP capable SoC with deterministic L2 cache.

Participants

Cyril Jean - Director, Embedded Systems Solutions, Microsemi, a Microchip company

Embedded Intelligence Everywhere

1:10pm - 1:30pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

2018 saw the rapid proliferation of the RISC-V architecture with commercial deployments of SiFive Core IP ranging from consumer wearables to enterprise cores. Modern compute workloads are evolving and require the ability to scale performance on-demand and very often have real-time, deterministic requirements. Intelligence is moving from the enterprise core to the IoT edge and requires a diverse combination of compute, storage and acceleration.

SiFive Core IP is architected to enable heterogeneous compute and efficiency requirements of applications by providing a scalable portfolio of CPU IP which can be customized according to the application requirements. In this talk we will highlight SiFive's IP portfolio and how it embeds intelligent processing for a hyper-connected world of a trillion connected devices.

Participants

Jack Kang - Vice President of Product Marketing, SiFive

Exhibit Hall Open: 10AM - 7PM

1:10pm - 2:25pm
Expo

Location: 1st Floor, Exhibit Hall A-2 & A-3

Sophon Edge AI platform with RISC-V Processor

1:35pm - 1:55pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Room 203/204

AI has been evolving at an unprecedented speed for the past 2 years. To enhance AI on the edge, BITMAIN's Sophon Edge AI platform is not only equipped with 1TOP int8 computing power but also contains a RISC-V processor as the sensor hub connecting the outside world. We believe this unique platform will bring in many exciting and innovative applications to the AIOT space and continue to push forward the development of the greater RISC-V architecture.

Participants

Speaker: Ian Chen - Product Marketing Director, Bitmain

NVIDIA's Deep Learning Accelerator meets SiFive's Freedom Platform

1:35pm - 1:55pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

In this talk, we introduce an open-source RISC-V-based SoC platform for edge inference applications based on NVIDIA Deep Learning Accelerator (NVDLA), NVIDIA's open-source inference engine, and SiFive's Freedom platform. NVIDIA has open-sourced its NVDLA initiative to address the computational demands of inference. NVIDIA's latest automotive SoC, Xavier, has incorporated two instances of the NVDLA. SiFive has open-sourced its Freedom platform, based on the RISC-V ISA, to quickly and cost effectively customize and add features for individual customers, unleashing the flexibility and power of custom silicon to the smallest company, inventor, and maker. SiFive has built FE310 and FU540 SoCs based on the Freedom platform, and has released HiFive1 and HiFive Unleashed development boards. NVIDIA and SiFive will jointly demo the NVDLA on the Freedom platform, and show the capabilities of the open-source edge inference platform.

Participants

Yunsup Lee - CTO, SiFive

Frans Sijstermans - Vice President Multimedia Arch/ ASIC, NVIDIA

SESSIONS

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

Formal Methods Need Not Be Black Magic

1:35pm - 1:55pm
Secure RISC-V

Location: 2nd Floor Meeting Rooms 209/210

We present R&D in creating new formal verification tools to support hardware design languages, and Bluespec SystemVerilog in particular. We focus on "Secret Ninja Formal Methods": creating powerful formal tools that behave like compilers usable by normal engineers. Our tools perform static reasoning about user-defined properties of designs and implementations, in all environments, under arbitrary conditions. They are also able to reason about software, firmware, and hardware within the same framework, and thereby provide a system-wide assurance case. Finally, and perhaps most critically, our tools are completely transparent and can provide evidence, both mathematical and practical -- a sharp contrast to the "formal" tools available in the EDA market today. In our talk, we will also provide some technical details about the core of our tools, highlight their strengths and weaknesses, and review several case studies.

Participants

Joseph Kiniry - Principal Scientist, Galois

Daniel Zimmerman - Principal Scientist, Galois

Analyzing the Disruptive Impact of a Silicon Compiler

2:00pm - 2:20pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Rooms 203/204

The complexity of chips has rapidly increased in line with the predictions of Moore's law. Recent years have seen an explosion in the cost and time require to design advanced System-on-Chips (SoCs), systems-in-packages (SiPs), and PCBs. DARPA is addressing these challenges through two new electronic design automation (EDA) research programs: the Intelligent Design of Electronic Assets (IDEA) program and the Posh Open Source Hardware (POSH) program. These programs seek to form the foundation of an intelligent hardware compiler. The aim of these research efforts is to create a universal hardware compiler capable of automatically generating production ready GDSII drawings directly from source code and schematics -- essentially developing the equivalent of a software compiler. Achieving this ambitious goal will require advancing the state of the art in machine learning, optimization algorithms, and expert systems. This talk will provide an overview of the recently announced DARPA POSH and IDEA research programs and present economic and societal disruption enabled by an open source SoC design ecosystem and no human in the loop silicon compilers.

Participants

Andreas Olofsson - Program Manager, DARPA

SiFive Freedom Revolution: Customizable RISC-V AI Platform with HBM2 and 56-112Gb/s SerDes

2:00pm - 2:20pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

The current interest in high-performance machine-learning processors has led to a demand for very high-bandwidth memory systems and high-speed chip-chip communication links. We have developed a RISC-V-based AI platform including RISC-V cores with vector extensions, HBM2 high-bandwidth memory interfaces, and Interlaken chip-chip interconnects carrying the TileLink coherence protocol. The HBM2 and 56Gb/s SerDes interfaces are silicon-proven in a 16nm FinFET technology demonstrator, with upcoming support for next-generation nodes. The platform can be configured with a variety of RISC-V management and compute cores, optimized on-chip cache and scratchpad memory systems, and customer-specific hardware acceleration blocks, and is supported with a full system software stack.

Participants

Krste Asanovic - Professor / Chief Architect, UC Berkeley | SiFive

A FIPS140-2 Compliant Trust Module for Quad 64-bit RISC-V Core Complex

2:00pm - 2:20pm
Secure RISC-V

Location: 2nd Floor Meeting Rooms 209/210

Cryptospec is an isolated trust module macrocell deeply embedded in 64-bit RISC-V system. Cryptospec protects sensitive information from unauthorized access. Its EEPROM/Flash/OTP serves as a storage for long-term, permanent keys such as RSA/DSA/ECDSA private keys as well as 3DES/AES/HMAC keys. Short-term keys such as TLS session keys 3DES/AES/HMAC keys are stored in RAM, and privacy related information in EEPROM/Flash. It prevents running unauthorized software based on go-or-no-go decision to CPU based on trust measure of the executing instructions/data. It also protects communication with outside world. Cryptospec has its own SSL/TLS or other secure communication mechanism which can exist in parallel with ones running on RISC-V system. Cryptospec OS runs on Cryptospec hardware offering two APIs, a packet API which enables outside on-chip CPUs to talk to Cryptospec, and another API which user download applets can link to.

Compared to prior secure elements with 1-bit serial interface, Cryptospec's hardware interface with RISC-V Coreplex configured to fit RISC-V coreplex system bus. Cryptospec can invoke interrupts for each of RISC-V cores. RISC-V cores can invoke Cryptospec interrupt. Cryptospec library includes plethora of asymmetric can symmetric cryptographic functions, which can be securely linked to user applets downloaded, and used by Cryptospec's encrypted download, communication, and system functions. Cryptospec will be fabricated along with quadcore bi-endian 64-bit RISC-V coreplex system and is certificable at the level of FIPS140-2 Level 3 federal government procurement standard. Cryptospec contains two 32-bit SH-2 MCUs with 2-stage pipeline with compact critical timing paths.

Participants

Shumpei Kawasaki - CEO, SH Consulting KK

Cong-Kha Pham - Professor, University of Ellectro-Communication

SESSIONS

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

UVM-based RISC-V Processor Verification Platform

2:25pm - 2:45pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Rooms 203/204

The momentum of the RISC-V ecosystem has spawned an increasing number of complex RISC-V processors by both commercial companies and the open source community. As these processor core designs grow in complexity, verification will continue to be the key challenge to delivering RISC-V processors that have robust functionality and meet target performance. In the open-source world, riscv-tests and riscv-torture have been widely used to verify RISC-V processors. These tests provide the necessary foundation to verify compliance to the ISA, but are not sufficient to address the verification challenges of complex processors.

In this session, we propose a comprehensive RISC-V verification platform (RISCV-VP) built with industry standard SystemVerilog (SV) and Universal Verification Methodology (UVM). The core of RISCV-VP is a SV/UVM-based random RISC-V assembly instruction generator, which supports many advanced features including full RISC-V privileged mode, page table randomization, page fault injection, nested loop structures, large numbers of sub-programs, CSR testing, and MMU stress testing. This instruction generator currently supports RV32IMC and RV64IMC subsets of the ISA. It can be easily extended to support other RISC-V instruction extensions. In addition to the instruction generator, RISCV-VP also provides useful components such as an interrupt agent, a debug agent, and a functional coverage monitor. We tested three open source RISC-V processors with RISCV-VP, ETH's RI5CY, Ariane plus a third 32b core. We present results that show how easily this framework integrates these processors and achieves much higher code and functional coverage compared with other open source verification flows. The framework found numerous bugs in the designs tested that were not found with other in-house or open-source verification flows, including in both datapath and control units.

Participants

Tao Liu - Senior Hardware Engineer, Google

Richard Ho - Principal Hardware Engineer, Google

Hwacha: A Data-Parallel RISC-V Extension and Implementation

2:25pm - 2:45pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

This talk describes the architecture and implementation of Hwacha, a scalable data-parallel accelerator focused on improving energy efficiency while remaining a favorable compiler target. Inspired by classical vector machines such as the Cray-1, as well as lessons learned from our previous vector-thread architectures Scale and Maven, Hwacha introduces the vector-fetch architectural paradigm: Vector instructions are hoisted into a separate thread to enable more aggressive access/execute decoupling of the vector data stream. Hwacha has been developed as a RISC-V non-standard extension (ISA string Xhwacha) block that attaches to the RoCC (Rocket Custom Coprocessor) interface. Several VLSI implementations have been taped-out in 16 nm, 28 nm, and 45 nm technology nodes at 1 GHz+ clock frequencies. Preceding this talk will be the open-source release of the ver- sion 4 RTL, compiler toolchain, and simulation and verification infrastructure, including FireSim AWS FPGA integration. Future iterations will transition to the proposed RISC-V V extension and feature 2D vector support based on vtype polymorphism.

Participants

Colin Schmidt - Graduate Student, UC Berkeley

Albert Ou - Graduate Student, UC Berkeley

Architecture Design Space Exploration Using RISC-V

2:25pm - 2:45pm
Secure RISC-V

Location: 2nd Floor Meeting Rooms 209/210

In this session, we discuss our work to develop a parameterized set of modules for design space exploration for RISC-V ISA based architectures. We introduce a design tool with:

- Multiple RISC-V cores with different levels of complexity (e.g., single-cycle core, multiple-cycle, and reconfigurable pipelined)
- A programmable memory system with reconfigurable multilevel cache subsystems
- A flexible interconnect network supporting programmable topology, router size and routing algorithm.

The aim of this work is to provide an easy to use, open-source, parameterized, fully synthesizable platform for students and researchers experimenting with the RISC-V ISA features to quickly bring up a complete and fully working architecture and start applying their own modifications.

Participants

Donato Kava - Graduate Student, Boston University

Sahan Bandara - Graduate Student, Boston University

RISC-V Linux Hackathon: 10AM - 7PM

2:25pm - 3:40pm
Expo

Don't miss out on the RISC-V Linux Hackathon, happening Dec. 4-5 on the Expo Floor at the RISC-V Summit.

Watch as a team of 10 expert hackers create cutting edge applications on a soft RISC-V CPU running Linux on the low-cost Avalanche FPGA board. Thanks to Western Digital for organizing!

Using the RISC-V PMP with an Embedded RTOS to Achieve Process Separation and Isolation

2:50pm - 3:10pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Rooms 203/204

The Physical Memory Protection (PMP) available on RISC-V cores is hardware that limits the access to memory and peripheral devices to only the code that needs to access those resources. The PMP allows an application developer to create more robust, safe and secure applications. The application can be organized by processes, each having access to its own memory and peripheral space. Not only does the PMP prevent application code from accessing memory or peripheral devices outside its designated area but, it can also be used to detect stack overflows. In this lecture, we will show how the PMP can interact with an RTOS and what recourses an RTOS has when a memory or I/O access violation is detected.

Participants

Jean Labrosse - Software Architect, Micrium / Silicon Labs

SESSIONS

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

Embracing a System-Level Approach in the Real World: Combining Arm & RISC-V in a Heterogeneous Designs

2:50pm - 3:10pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

RISC-V is gaining substantial market traction; in the process the ecosystem's focus is moving from purely legacy/incumbent processor-centric thinking to system-level issues. Part of that move is a growing realization that many, if not most, designs will include RISC-V, *in addition to* other CPUs and GPUs, rather than as a system-wide substitute. Issues of heterogeneous design, therefore become key architectural considerations. In addition there needs to be an infrastructure that supports the co-existence of legacy subsystems with new ones such as those implemented using RISCV. An "ecosystem on chip" should be developed as system: not as though it were a collection of independent pieces. This presentation will look at these issues and how they can be addressed. We will provide specific examples, focusing particularly on designs that combine RISC-V and Arm processors within the same SoC.

Participants

Gajinder Panesar - CTO, UltraSoC

Making RISC-V The Most Secure Platform

2:50pm - 3:10pm
Secure RISC-V

Location: 2nd Floor Meeting Rooms 209/210

In this session industry veteran Cesare Garlati, long time supporter of the RISC-V Foundation and active member of the RISC-V Security Group, will share the latest on RISC-V security and will offer his practitioner advice for developing secure applications. Garlati will start with an explanation of the security building blocks defined by the ISA including privileged modes and physical memory protection. He will then show how to combine these blocks to develop trusted applications with particular emphasis on IoT devices that lack MMU – and this is where the audience will be surely impressed with the capabilities of RISC-V. Finally, Garlati will introduce a breakthrough system design philosophy, entirely based on free and open standards, that allows hardware-enforced software-defined separation of data, programs and peripherals for an unlimited number of trusted execution environments. This session will appeal to anyone with an interest in embedded security in general and in RISC-V in particular: from SoC designers to hardware and software architects to OEMs and system integrators.In this session industry veteran Cesare Garlati, long time supporter of the RISC-V Foundation and active member of the RISC-V Security Group, will share the latest on RISC-V security and will offer his practitioner advice for developing secure applications. Garlati will start with an explanation of the security building blocks defined by the ISA including privileged modes and physical memory protection. He will then show how to combine these blocks to develop trusted applications with particular emphasis on IoT devices that lack MMU – and this is where the audience will be surely impressed with the capabilities of RISC-V. Finally, Garlati will introduce a breakthrough system design philosophy, entirely based on free and open standards, that allows hardware-enforced software-defined separation of data, programs and peripherals for an unlimited number of trusted execution environments. This session will appeal to anyone with an interest in embedded security in general and in RISC-V in particular: from SoC designers to hardware and software architects to OEMs and system integrators.

Participants

Cesare Garlati - Co-Founder, Hex Five Security

Networking Break

3:10pm - 3:40pm
Open RISC-V Platforms

Networking Break

3:10pm - 3:40pm
RISC-V Accelerators

Networking Break

3:10pm - 3:40pm
Secure RISC-V

A Processor Description Language Optimized for RISC-V

3:40pm - 4:00pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Rooms 203/204

As the RISC-V ISA specification evolves and adds an ever-increasing number of optional architecture extensions, a processor design methodology that allows for both rapid architectural exploration and simplified creation of easily implementable RTL becomes essential. What is needed is a high-level processor description language optimized for RISC-V. The presentation will demonstrate how the new and enhanced Codasip Studio 8 was used to (a) create a new 64-bit RISC-V processor implementation and (b) to perform design exploration around the emerging B and P standard extensions. Additionally, it will introduce the following new Studio and software tool functionality:

- Support for LLVM debugger (LLDB) and OpenOCD
- LLVM 7.0
- Studio/CodeSpace IDEs based on Eclipse Oxygen, along with more interactive consoles
- Improved test suites and verification to better support user-defined RISC-V extensions.

Participants

Zdenek Prikryl - CTO, Codasip

SESSIONS

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

Massively Parallel RISC-V Processing with Transactional Memory

3:40pm - 4:00pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

There are myriad architectures for multiple core processing systems and their memories, which vary greatly and are highly tuned to the application. In the past such systems have had bespoke processors or standard processors shoe-horned in. The advent of an open processor instruction set architecture in RISC-V provides an exciting new opportunity to address a broad range of embedded processing applications with tailored optimizations and instruction customizations.

A major differentiation between architectures will be in the memory hierarchy and capabilities; general purpose processors drive toward coherent caches to maximize CPU performance using temporal locality; DSPs stream data; GPUs have texture caches and separate processor memories. In some processing applications, it is beneficial to have a transactional memory hierarchy, with high bulk bandwidth and a lot of support in the memories for operations such as "look up a value and add it to a table". Such operations do not necessarily marry well to a load/store CPU architecture, and the performance of a system will tend to be limited by the number of memory transactions per second as well as CPU cycles; this latter issue encourages memory-centric processing, and hence the latency for transactions from a processor may be high (perhaps even over a hundred cycles). To cover this latency and achieve high silicon efficiency requires a lot of CPU threads, and suitable sharing of CPU resources.

In this talk, we discuss some of the background, and describe the example of a thousand RISC-V harts performing the processing required in a SmartNIC. We show how a RISC-V solution can be tailored with a suitable choice of instruction set features, privilege modes and debug methodology; we cover at a high level the organization of memories and RISC-V harts that provides efficient processing with high latency memory transactions; we look at the instruction set customizations that allow this to handle RISC-V hart interaction with the memory systems and other harts; and we show how this applies in an example.

Participants

Steve Zagorianakos - Distinguished Engineer and Vice President, Engineering, Netronome

Panel: RISC-V Security Ecosystem: Open for Business

3:40pm - 4:20pm
Secure RISC-V

Location: 2nd Floor Meeting Rooms 209/210

The RISC-V ISA defines some key building blocks for secure computing including privileged modes and crypto extensions. However, commercial implementations may not include these standard extensions or provide vendor-specific architectures requiring additional non-standard specialized hardware. For system designers, security is seldom a differentiating feature and often added late in the development cycle to a predefined architecture. History shows that many security implementations fail due to an excess of complexity and an inability to verify the fully integrated solution – when they fail, there is a real risk that the blame will affect the RISC-V brand as a whole rather than the specific faulty implementation.

As RISC-V commercialization proceeds, many aspects of its ecosystem are now “Ready for Business” but there has not been a discussion of the commercial readiness of the security segment. This enlightening panel will cover the RISC-V security issues faced by a customer during implementation, discuss several commercial solutions to secure RISC-V and cover holistic test & verification best practices at the platform level.

Participants

Moderator: Brandon Lewis - Editor-in-Chief, Embedded Computing Design, OpenSystems Media

Panelist: Chuanhua Chang - Senior director of RD/ Architecture Division, Andes Technology

Panelist: Cesare Garlati - Co-Founder, Hex Five Security

Panelist: Jothy Rosenberg - CEO & Founder, Dover Microsystems

Panelist: Martin Scott - SVP & GM, Rambus

Exhibit Hall Open: 10AM - 7PM

3:40pm - 4:35pm
Expo

Location: 1st Floor, Exhibit Hall A-2 & A-3

Making a Complex, Linux-enabled SoC Available to Everyone Today with Renode

4:05pm - 4:35pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Rooms 203/204

Universal availability of mainstream Linux-capable SoCs is a major milestone for RISC-V. A multi-core, Linux-capable RISC-V SoC will be unveiled at the Summit, the first mainstream, widely available, powerful and flexible RISC-V SoC product from a major vendor. To get the platform into the hands of developers worldwide without limitations, support for the SoC was developed by Antmicro in the free and open source Renode framework. This includes not only the CPU but the entire SoC, also providing the possibility to connect external elements like virtual sensors as well as other SoCs/boards, allowing users to simulate production software for their products while waiting for silicon to be available. Additional collaboration features of Renode, its integration with continuous integration and testing frameworks will further enhance this revolutionary simulator-first workflow that will be described in this presentation.

Participants

Michael Gielda - VP Business Development, Antmicro

Accelerating Computational Storage Over NVMe with RISC-V

4:05pm - 4:25pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

With the vast amount of data being generated and stored on SSD, the limited network bandwidth is the bottleneck for processing this data. Therefore, compute must move closer to where the data resides. In this talk, we will show how Eideticom's NoLoad NVMe accelerators running on SiFive's RISC-V platforms enable a seamless method for running your applications directly on the storage server, with minimal impact on the host CPU and network resources.

Participants

Stephen Bates - CTO, Eideticom

SESSIONS

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

AI at the Edge Using PULP + eFPGA

4:30pm - 4:50pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

PULP is a silicon-proven open-source parallel platform for ultra-low power computing created by researchers at ETHZ and UNIBO with the objective of delivering high compute bandwidth combined with high energy efficiency. The platform is organized in clusters of RISC-V cores that share a common and tightly-coupled data memory subsystem. The platform also includes a set of System Verilog-described IP blocks, their related synthesis and simulation scripts, and the runtime software (written in C and RISC-V assembly) necessary to provide a complete system. All of the architecture, IP, scripts and software are open sourced to encourage global collaboration and development.

Integrating eFPGA technology with the PULP Platform enables users to offload critical functions from the processor(s) and implement them in eFPGA fabric. This approach enables the creation of multiple hardware co-processors that increase system efficiency and performance while decreasing power consumption. An example use case for the eFPGA technology is to enable hardware acceleration of feature extraction for AI applications. In this case, using eFPGA fabric significantly improves performance and lowers power consumption by offloading those functions from the RISC-V processor while still maintaining the ability to adopt and implement new algorithms even after field development. Our goal is to implement AI at the edge in a single platform with reconfigurable acceleration capabilities; for this purpose, ETH and QuickLogic are developing a test chip in 22FDX technology which will showcase the benefits of having AI feature extraction implemented in eFPGA fabric to achieve higher performance with the lowest possible power consumption.

Participants

Timothy Saxe - CTO & SVP Engineering, QuickLogic

Luca Benini - Professor, ETH Zurich

RISC-V MultiCore Secure Boot

4:30pm - 4:50pm
Secure RISC-V

Location: 2nd Floor Meeting Rooms 209/210

Security has emerged as the preeminent concern in architecting and designing Embedded Systems in broad deployment today for mission critical applications, where higher levels of reliability and tamper-resistance are fundamental requirements. The process of booting Linux on an SOC involves multiple stages before transferring control to the Linux Kernel. After Reset is applied, a First Stage Boot Loader (FSBL) pointed to by the Reset Vector is invoked. FSBL is typically stored in on-chip NVM which is protected by a few layers of security restricting access privileges. As the methods of attack are becoming more sophisticated, this approach is deemed inadequate to guard against a scenario where a malicious agent manages to alter the FSBL. We present here Secure Boot of SOC advanced security capabilities: Before the FSBL is executed, a “Zero Stage Boot Loader” (ZSBL) is pushed into the SOC by the “Root of Trust” for the purpose of authenticating the NVM image before transferring control to FSBL. A Secure Hash Algorithm (SHA) of NVM image is run on the RV64G cores included in the SOC. The calculated hash is then checked against a purported value in a signed code certificate for FSBL. Choice of SHA512/256 was made to take advantage of 64-bit compute and managed to speed up the operation by partitioning the workload over 2 Cores.

Participants

Pierre Selwan - Chief Architect, Microsemi, a Microchip company

Ken Irving - Chief Engineer, Microsemi, a Microchip Company

RISC-V Linux Hackathon

4:35pm - 5:30pm
Expo

Don't miss out on the RISC-V Linux Hackathon, happening Dec. 4-5 on the Expo Floor at the RISC-V Summit.

Watch as a team of 10 expert hackers create cutting edge applications on a soft RISC-V CPU running Linux on the low-cost Avalanche FPGA board. Thanks to Western Digital for organizing!

Extending the RISC-V ISA for Optimized Support of CNNs in a Multi-Core Context

4:55pm - 5:25pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

Extensibility is in integral part of the RISC-V Instruction Set Architecture (ISA). The decision to extend the ISA in a particular way is mostly influenced by few highly structuring hypotheses rooted in the application domain(s) for which a performance boost is required. The motivation for such a boost can be faster execution but it can also at same time be directed towards reducing power consumption.

One of the challenges posed by extensions is how to preserve balanced characteristics of the micro architecture used: gate cost, critical paths, ... GAP8 leverages the PULP open source initiative which is itself using the RISC-V ISA for its processing elements. Both PULP and GAP8 are heavily using RISC-V extensions.

In this session, we will show how these extensions are bringing a significant performance/energy boost compared to the base RISC-V ISA for Deep/Convolutional Neural Network (DNN/CNN) applications by combining Digital Signal Processing (DSP) related extensions with advanced Single Instruction Multiple Data (SIMD) capability. We will go step by step through the optimization process that led to the ISA extension definition. We will then show how such an extended core can be used efficiently in a multiple core shared memory model still using CNN/DNN applications as a driving use case. We will illustrate the capability of the GAP8 multiple core SoC on some real-life medium complexity CNNs.

Participants

Eric Flamand - CTO, GreenWaves Technologies

Functional Safety and Security, ISO26262, and Their Implications for the RISC-V Ecosystem

4:55pm - 5:25pm
Secure RISC-V

Location: 2nd Floor Meeting Rooms 209/210

ISO26262 is becoming very important for the semiconductor industry, as it is an entry requirement for many automotive and safety-critical applications which represent a massive opportunity for the RISC-V community. But the risk connected to the use of RISC-V is still regarded as high especially when used for a S/W intensive application. In this context, monitoring software execution and potential anomalies is increasingly important in order to address

- systematic faults in the design (software or hardware bugs)
- run-time failure of the system
- deliberate interference

This can be achieved with a minimum overhead (hardware and software) in a non-intrusive way and with easy instrumentation. This presentation will cover these fundamental concepts and discuss hardware and software FuSa features across the entire SoC.

Participants

Gajinder Panesar - CTO, UltraSoC

Marco Demi - Senior Safety Engineer, ResilTech

Happy Hour on the Expo Floor

5:30pm - 7:00pm

Innovation Celebration

7:00pm - 10:00pm

Hosted by Martin Fink, CTO of Western Digital, Naveed Sherwani, CEO of SiFive, and the co-founders of RISC-V, you are invited to join with fellow innovators at the Hyatt Regency Santa Clara Hotel Grand Ballroom, December 4th from 7:00 pm - 10:00 pm. Featuring world-renowned performance painter, Garibaldi, we are celebrating innovation, both past and that yet-to-come from RISC-V, while being entertained with dazzling displays of creativity, music, drinks, and food.

Space is limited so be sure to RSVP* as soon as possible. Click here to register for the event.

*Must hold an All Access, Conference or Preconference pass for the RISC-V Summit to attend. Exhibition-only passes are not eligible.

SCHEDULE

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

RISC-V Summit

December 3 - 6, 2018
Santa Clara Convention Center
Santa Clara, CA

TIME	BIRDS OF A FEATHER	EXPO	KEYNOTES	MAIN AGENDA	OPEN RISC-V PLATFORMS	RISC-V ACCELERATORS	SECURE RISC-V
8:00AM			**8:00am** - Registration Open: 7:30 AM - 6:30 PM **8:20am** - Welcome & RISC-V ISA & Foundation Overview **8:40am** - RISC-V State of the Union				
9:00AM			**9:10am** - Unleashing Innovation from Core to Edge **9:40am** - Enabling the Freedom to Innovate				
10:00AM		**10:00am** - Exhibit Hall Open: 10AM - 7PM **10:50am** - RISC-V Linux Hackathon: 10AM - 7PM	**10:00am** - Networking Break				
11:00AM		**11:40am** - Expo Hall Open 10:00 AM - 7:00 PM	**11:00am** - The 100X Problem – How to Redefine Silicon for Augmented Reality	**11:40am** - Lunch & Exhibit Hall Visit			
12:00PM	**12:00pm** - Birds of Feather Discussion: Debugging + Tracing	**12:25pm** - RISC-V Linux Hackathon: 10AM - 7PM					

SCHEDULE

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

TIME	BIRDS OF A FEATHER	EXPO	KEYNOTES	MAIN AGENDA	OPEN RISC-V PLATFORMS	RISC-V ACCELERATORS	SECURE RISC-V
1:00PM		**1:10pm** - Exhibit Hall Open: 10AM - 7PM			**1:10pm** - CPU Project in Western Digital: From Embedded Cores for Flash Controllers to Vision of Datacenter Processors with Open Interfaces **1:35pm** - Sophon Edge AI platform with RISC-V Processor	**1:10pm** - Deterministic L2 Cache Solution and Performance in an AMP capable SoC **1:35pm** - NVIDIA's Deep Learning Accelerator meets SiFive's Freedom Platform	**1:10pm** - Embedded Intelligence Everywhere **1:35pm** - Formal Methods Need Not Be Black Magic
2:00PM		**2:25pm** - RISC-V Linux Hackathon: 10AM - 7PM			**2:00pm** - Analyzing the Disruptive Impact of a Silicon Compiler **2:25pm** - UVM-based RISC-V Processor Verification Platform **2:50pm** - Using the RISC-V PMP with an Embedded RTOS to Achieve Process Separation and Isolation	**2:00pm** - SiFive Freedom Revolution: Customizable RISC-V AI Platform with HBM2 and 56-112Gb/s SerDes **2:25pm** - Hwacha: A Data-Parallel RISC-V Extension and Implementation **2:50pm** - Embracing a System-Level Approach in the Real World: Combining Arm & RISC-V in a Heterogeneous Designs	**2:00pm** - A FIPS140-2 Compliant Trust Module for Quad 64-bit RISC-V Core Complex **2:25pm** - Architecture Design Space Exploration Using RISC-V **2:50pm** - Making RISC-V The Most Secure Platform
3:00PM		**3:40pm** - Exhibit Hall Open: 10AM - 7PM			**3:10pm** - Networking Break **3:40pm** - A Processor Description Language Optimized for RISC-V	**3:10pm** - Networking Break **3:40pm** - Massively Parallel RISC-V Processing with Transactional Memory	**3:10pm** - Networking Break **3:40pm** - Panel: RISC-V Security Ecosystem: Open for Business

SCHEDULE

CONFERENCE DAY 1, DECEMBER 4, 2018 - 04/12/2018

TIME	BIRDS OF A FEATHER	EXPO	KEYNOTES	MAIN AGENDA	OPEN RISC-V PLATFORMS	RISC-V ACCELERATORS	SECURE RISC-V
4:00PM		**4:35pm** - RISC-V Linux Hackathon			**4:05pm** - Making a Complex, Linux-enabled SoC Available to Everyone Today with Renode	**4:05pm** - Accelerating Computational Storage Over NVMe with RISC-V **4:30pm** - AI at the Edge Using PULP + eFPGA **4:55pm** - Extending the RISC-V ISA for Optimized Support of CNNs in a Multi-Core Context	**4:30pm** - RISC-V Multi-Core Secure Boot **4:55pm** - Functional Safety and Security, ISO26262, and Their Implications for the RISC-V Ecosystem
5:00PM	**5:30pm** - Happy Hour on the Expo Floor	**5:30pm** - Happy Hour on the Expo Floor	**5:30pm** - Happy Hour on the Expo Floor	**5:30pm** - Happy Hour on the Expo Floor	**5:30pm** - Happy Hour on the Expo Floor	**5:30pm** - Happy Hour on the Expo Floor	**5:30pm** - Happy Hour on the Expo Floor
6:00PM							
7:00PM	**7:00pm** - Innovation Celebration	**7:00pm** - Innovation Celebration	**7:00pm** - Innovation Celebration	**7:00pm** - Innovation Celebration	**7:00pm** - Innovation Celebration	**7:00pm** - Innovation Celebration	**7:00pm** - Innovation Celebration

SESSIONS

CONFERENCE DAY 2, DECEMBER 5, 2018 - 05/12/2018

Registration Open: 8:00 AM - 5:30 PM

8:00am - 8:25am
Keynotes

Welcome

8:25am - 8:30am
Keynotes

A New Golden Age for Computer Architecture: History, Challenges, and Opportunities

8:30am - 9:00am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

In the 1980s, Mead and Conway democratized chip design and high-level language programming surpassed assembly language programming, which made instruction set advances viable. Innovations like Reduced Instruction Set Computers (RISC), superscalar, and speculation ushered in a Golden Age of computer architecture, when performance doubled every 18 months. The ending of Dennard Scaling and Moore's Law crippled this path; microprocessor performance improved only 3% last year!

The ending of Dennard scaling and Moore's law and the deceleration of performance gains for standard microprocessors are not problems that must be solved but facts that if accepted offer breathtaking opportunities. We believe high-level, domain-specific languages and architectures and freeing architects from the chains of proprietary instruction sets will usher in a new Golden Age. Aided by open source ecosystems, agilely developed chips will convincingly demonstrate advances and thereby accelerate commercial adoption. The instruction set philosophy of the general-purpose processors in these chips will likely be RISC, which has stood the test of time. We envision the same rapid improvement as in the last Golden Age, but this time in cost and energy as well as in performance.

Like the 1980s, the next decade will be exciting for computer architects in academia and in industry!

Participants

David Patterson - Vice Chair, RISC-V Foundation

Opportunities and Challenges of Building Silicon in the Cloud

9:00am - 9:20am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Yunsup Lee - CTO, SiFive

Deepening the RISC-V Ecosystem to Drive Industry-Wide Adoption

9:20am - 9:40am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Rob Oshana - Co-Chair, Program Committee | VP Software Engineering, NXP

Accelerating Innovation: Why Google's TPU Was Just the Start

9:40am - 10:00am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Michael Gielda - VP Business Development, Antmicro

Networking Break on the Expo Floor

10:00am - 10:40am
Keynotes

Exhibit Hall Open: 10AM - 3:30PM

10:00am - 10:15am
Expo

Location: 1st Floor, Exhibit Hall A-2 & A-3

RISC-V Linux Hackathon: 10AM - 3:00PM

10:15am - 12:35pm
Expo

Don't miss out on the RISC-V Linux Hackathon, happening Dec. 4-5 on the Expo Floor at the RISC-V Summit.

Watch as a team of 10 expert hackers create cutting edge applications on a soft RISC-V CPU running Linux on the low-cost Avalanche FPGA board. Thanks to Western Digital for organizing!

Keynote Panel: Opportunities and Challenges in Security for Open Source Hardware

10:40am - 11:20am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Since the publication of the devastating Spectre and Meltdown attacks on Intel and ARM processors earlier this year, closely followed by Ryzenfall on AMD processors, the computer architecture community has woken up to the very real threats this new generation of side-channel attacks represent for proprietary processor designs and instruction set architectures. On the other end of the spectrum, the open source hardware community has been working on bringing the RISC-V instruction set architecture into the public domain and created its own foundation to move open source hardware principles forward. That community too has recently woken up to the urgency of addressing security issues and to the question of how to build secure processors based on its open instruction set. This panel of recognized security experts will discuss:

- some of the newly emerging threats on processors such as the newest TLBleed, speculative buffer overflow and timing side-channel attacks which yet again show how vulnerable processors are to side-channel attacks.
- some of the advantages of the RISC-V approach to counter these types of threats,
- which particular threats may still be a concern even for RISC-V processors beyond the traditional proprietary processor architectures.
- work that has been undertaken by the RISC-V Foundation to add security features and relevant extensions to the RISC-V instruction set architecture to start aligning RISC-V processing with the required security extensions, basic building blocks and primitives required for secure execution.

Participants

Moderator: Ed Sperling - Editor In Chief, Semiconductor Engineering

Panelist: Helena Handschuh - Chair of the RISC-V Foundation Security Standing Committee | Fellow, Rambus

Panelist: Joseph Kiniry - Principal Scientist, Galois

Panelist: Richard Newell - Senior Principal Product Architect, Microsemi, a Microchip Company

RISC-V: Opportunities and challenges in SoCs

11:20am - 11:40am
Keynotes

Location: 1st Floor, Exhibit Hall A-1

Participants

Greg Wright - Sr. Director, Engineering, Qualcomm Technologies, Inc.

SESSIONS

CONFERENCE DAY 2, DECEMBER 5, 2018 - 05/12/2018

Lunch

11:40am - 1:10pm
Keynotes

Running Other Architecture Operating Systems and Applications on RISC-V Using QEMU

1:10pm - 1:30pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Room 203/204

QEMU allows running an operating system compiled for a different architecture on the current architecture. This is commonly used to develop and debug embedded systems (such as ARM architectures) on Intel workstations (x86). Currently mainline QEMU supports RISC-V guests, allowing development and debugging of RISC-V operating systems on Intel machines. This presentation focuses on allowing x86 operating systems to run on the RISC-V architecture using QEMU. It also discusses the work involved in upstreaming the implementation. Using this we can run the first instance of QEMU to emulate a RISC-V machine on an x86 workstation. We can then start a second QEMU instance inside the first one to run x86 operating systems on top of the RISC-V machine. The same setup can be used on a real RISC-V board.

Participants

Alistair Francis - Principal Engineer, Western Digital

Domain-Specific Acceleration via AndeStar V5 Processors

1:10pm - 1:30pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

Application-Specific Instruction Processors (ASIP's) or Purpose-Built Accelerators have been popular for years in applications where performance is demanding, and cost and power are sensitive. As Moore's Law approaches the end of its life, DSA (Domain-Specific Architecture) becomes even more important to continue to carry the ever-increasing computing demands forward.

In this talk, we will:

- Give an update of Andes V5 processor solutions.
- Introduce a comprehensive solution to unlock the potential DSA in RISC-V.
- Explain how a powerful tool COPILOT greatly simplifies design and verification of advanced custom instructions.
- Use practical examples to demonstrate how our solutions help solving real-world problems.

Participants

Charlie Su - CTO and SVP of R&D, Andes Technology Corporation

If We Get RISC-V Security Right, It Will Become the Dominant Processor in the $470B IoT Market

1:10pm - 1:30pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

The IoT "cyber epidemic" is an existential threat to civilized society. We are dangerously vulnerable to this threat because bugs in software let attackers in, and defenseless processors do their bidding. This must be addressed in hardware at the processor level. With its low barriers to entry and no legacy requirements to support, we have a unique opportunity with RISC-V to truly fix this problem. We can protect a RISC-V core from network-based attacks --without changing it -- using three key innovations.

1. First, generate metadata about the intent of the application to provide a co-processor with information unavailable in today's standard development environments.
2. Second, apply a set of rules called micro-policies to describe the security properties we want to maintain and enforce.
3. And third, create simple but powerful hardware mechanism that watches every instruction, examines the critical metadata, and evaluates the aforementioned rules to block any instruction doing the wrong thing.

The RISC-V community is ideally suited to wield this revolutionary technology to create processors that can dominate the burgeoning IoT market, while making our connected world a safer and more secure place.

Participants

Jothy Rosenberg - CEO & Founder, Dover Microsystems

Exhibit Hall Open: 10AM - 3:30PM

1:10pm - 1:30pm
Expo

Location: 1st Floor, Exhibit Hall A-2 & A-3

RISC-V Linux Hacakthon: 10AM - 3:00PM

1:30pm - 3:00pm
Expo

Don't miss out on the RISC-V Linux Hackathon, happening Dec. 4-5 on the Expo Floor at the RISC-V Summit.

Watch as a team of 10 expert hackers create cutting edge applications on a soft RISC-V CPU running Linux on the low-cost Avalanche FPGA board. Thanks to Western Digital for organizing!

How to Address RISC-V Compliance in the Era of OPEN ISA and Custom Instructions

1:40pm - 2:00pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Room 203/204

One mission-critical task for the RISC-V SoC developers and implementors is the need to test and verify that RISC-V cores are compliant to the specifications, including user and privilege modes. The RISC-V market will depend on the wide and diverse availability of silicon devices that can leverage the investment in RISC-V software across all conforming devices. This is only possible when building on a foundation of devices with guaranteed compliance with the specifications. Many RISC-V chips, systems and design flows will exploit the concept of custom instructions or other optimizations, delivering unique features. In these cases especially, the need to continuously test and confirm compliance throughout the design process becomes essential for all RISC-V based SoCs and systems. The technical issues of determining compliance with the RISC-V ISA are introduced with examples of customer extensions. The question of completeness and specification coverage are discussed and use cases of tool usage is provided. The Imperas experience of examining compliance on various proprietary RTL, open source RTL, FPGA, silicon, and ISS models will be explained with issues experienced being explained. A methodology to ensure continuous compliance during the development process from initial modeling, early RTL through final silicon will be shown.

Participants

Simon Davidmann - CEO, Imperas

Lee Moore - Lead Engineer, Imperas

The Esperanto ET-Maxion High Performance Out-of-Order RISC-V Processor

1:40pm - 2:00pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

In this talk, we will present an update on ET-Maxion, a high frequency out-of-order RISC-V core which is being designed for TSMC's 7nm process. In the first part of our talk, we will describe its key micro-architectural features that allow it to achieve performance levels comparable to existing commercial high-end processors and discuss some of the design choices that we made. One such choice was the design of ET-Maxion as a core shielded against timing attacks such as Spectre and Meltdown. We will show that when such decisions are made early in the design process, they can be supported with negligible performance sacrifices. We will then share some of our experiences from implementing the RISC-V compressed instructions (RVC) and the weak consistency model (RV-WMO) in a superscalar out-of-order core, and present some of the design challenges we encountered. We will conclude our talk with a brief overview of our support for post-silicon debug and the performance monitoring improvements that we are planning to implement for ET-Maxion.

Participants

Polychronis Xekalakis - CPU Architect, Esperanto Technologies

Christopher Celio - CPU Architect, Esperanto Technologies

Never Again: Spectre-Proofing Chip Designs with End-to-End Formal Methods

1:40pm - 2:00pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

No one likes nasty surprises when microarchitectural optimizations combine to cause security problems, but how can we avoid those surprises without exhaustive consideration of all pairwise interactions between features in our chip designs? Formal methods provide a solution. Our team at MIT has been proving that concrete RISC-V designs avoid timing side channels, and the theorems apply to the end-to-end combination of hardware and software. For software implementations of widely used cryptographic algorithms, we prove that the timestamped history of signals on input and output wires is independent of changes to secret inputs. All proofs are checked algorithmically, so there is very little room for human error to endanger a security guarantee. We have designed a modular-decomposition strategy for security obligations, so that, for instance, each of a software program, a processor, and a memory system with caches can be analyzed separately. Then such components can be remixed to derive end-to-end theorems for new combinations with minimal new engineering effort. I will speculate (pun intended?) on how our initial results can scale to cover full-scale processors and reasonable mitigations to the Spectre and Meltdown attacks.

Participants

Adam Chlipala - Associate Professor, MIT

Accelerating Inferencing on the Edge with RISC-V

2:10pm - 2:30pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Room 203/204

Machine-learning algorithms are highly compute intensive. Inferencing, which may be done on embedded systems (edge nodes), is less compute intensive, but certain applications such as real-time video image processing may stress the capabilities of even the fastest embedded processors. One way to address this problem is to move parts of the inferencing algorithms into accelerators implemented in hardware.

This session will explore the use of high-level synthesis to create machine learning accelerators specific to an implementation to meet demanding power and performance goals. In traditional proprietary CPU architectures accelerators need to be accessed as peripherals. Much of the benefit of an accelerator is often lost through the time and energy needed to move the data in and out of the processor core. In contrast, RISC-V's open architecture allows developers to implement accelerators as more tightly integrated functions, as co-processors or even new instructions, delivering higher performance and lower power. This session will explore the impact of accelerators integrated into RISC-V cores in various ways.

Participants

Russell Klein - Technical Director, Mentor, A Siemens Company

Methodologies Behind the World's First RISC-V-based SSD Controller

2:10pm - 2:30pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

This talk will showcase the design, methodology, and results behind the world's first RISC-V based SSD controller: the FADU Annapurna PCIe 3.0 X 4 NVMe SSD controller. The FADU Annapurna provides high throughput (3.5GB) and IOPS (800K), while consuming less than 1.8W active power. Powered by the FADU Annapurna, the FADU Bravo SSD is the first 7mm low-power U.2 supporting dual port and offers 3-4X IOPS / watt greater efficiency, 30% lower power, and the most consistent latency QoS in its class while only consuming 6-8W of active power. This talk will describe the innovative design, advanced flash memory controller system, and use of high-performance 64-bit embedded RISC-V Core IP that achieved this. The successful use of RISC-V IP has important implications for SSD development, particularly in future hyperscale datacenter applications. The adoption of RISC-V has positive implications for optimizing for small form factors and managing thermal and power constraints on advanced nodes for memory applications. FADU achieves this by the advanced and innovative architecture, extensive HW automation, flash acceleration, off-loading, and bypassing to be showcased in this talk.

Participants

Jihyo Lee - CEO & Co-Founder, FADU

How to Protect RISC-V Against Side-Channel Attacks?

2:10pm - 2:30pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

Software implementations of cryptographic algorithms are vulnerable to Side-channel Analysis (SCA) attacks, basically relinquishing the key to the outside world through measurable physical properties of the processor like power consumption and electromagnetic radiation. Protected software implementations typically have a significant timing and code size overhead, as well as a substantially long development time because hands-on testing the result is crucial. Plenty of scientific publications offer solutions for this problem for all kinds of algorithms, but they are not straightforward to implement, as they rely on device assumptions which are rarely met, nor do these solutions take micro-architecture related leakages into account.

We present a solution to this problem by integrating side-channel analysis countermeasures into a RISC-V implementation. Our solution protects against any first-order power or electromagnetic attacks while keeping the implementation costs as low as possible. We made use of state-of-the-art masking techniques and present a novel solution to protect memory access against SCA. Practical results are shown that demonstrate the efficiency of various cryptographic primitives running on our protected hardware platform.

Participants

Elke De Mulder - Embedded Security Researcher, Rambus

Michael Hutter - Senior Principal Engineer, Rambus

Command-Driven Data Transfer Protocols in RISC-V SoCs

2:40pm - 3:00pm
Open RISC-V Platforms

Location: 2nd Floor Meeting Room 203/204

There has been substantial interest in data transfer and synchronization protocols in RISC-V based SoCs. The Freedom series of SoCs use the Tile Link Protocol for cache coherence across CPUs and accelerators. CCIX and OpenCAPI are two other protocols that have received substantial attention and development effort. More recently, the Gen-Z protocol aims to provide memory-semantic access to shared storage. In this talk, we propose that high-performance multi-core systems with hundreds of cores may also need a third kind of data management protocol: programmer-managed bulk- and atomic-data transfers. The talk will demonstrate how workloads can benefit from such a protocol. Netronome has previously used such a protocol for on-chip data transfers in implementing high-performance coprocessors for networking. We will explore how this protocol can potentially be extended to intra-chip transfers in chiplet-based systems. We will also discuss potential changes to the RISC-V instruction set to enable programmer-managed data transfers. Finally, we will discuss how this protocol may be implemented over a popular link layer, such as PCIe.

Participants

Rajesh Vaidheeswarran - Director of Engineering and Sr. Principal Architect, Netronome

Machine-Readable Specifications of RISC-V ISA

2:40pm - 3:00pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

In this talk, we discuss the use of machine-readable ISA specifications for creating verification tools for RISC-V microprocessors. Our team is working on the MicroTESK open-source verification framework. It uses machine-readable specifications in the nML language to automatically construct the following tools: an instruction set simulator, a test program generator, an online test program generator, and a binary code static analyzer. nML specifications describe registers, memory storages, addressing modes, and instructions' syntax and semantics. By the moment, the following RISC-V instruction subsets have been specified: RV32I, RV64I, RV32M, RV64M, RV32A, RV64A, RV32F, RV64F, RV32D, RV64D, and RVC. In total, the specifications cover about 250 instructions. The effort required to develop the specifications constituted about 4 person-months. The specifications can be easily modified to support more instructions (including custom extensions). The MicroTESK technology has been previously used to create TPGs for several RISC ISAs including ARMv8 and MIPS64, which have been successfully applied in industrial projects. The framework and the RISC-V ISA specifications are distributed under Apache License, Version 2.0.

Participants

Alexander Kamkin - Leading Researcher, ISP RAS

SiFive TERP: A Trusted Execution Reference Platform for Embedded Secure Applications

2:40pm - 3:00pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

The SiFive Trusted Execution Reference Platform (TERP) is an open source RISC-V reference architecture demonstrating a complete system which enables trusted execution of embedded security applications. The goal of TERP is to describe all the components necessary to build an embedded RISC-V processor which provides isolated multi-tenancy. We demonstrate that the resulting architecture is capable of supporting a wide array of target applications by evaluating multiple case-studies including operation of TERP as an asymmetric-key cryptography accelerator, a hardware random number generator, a Time-based One-Time Password (TOTP) token, a biometric identity verification card, and as a high-confidence command validation module. Finally, we have created a reference implementation of TERP as an FPGA image with firmware to demonstrate the use of TERP to build a USB hardware token for performing asymmetric-key cryptography.

Participants

Palmer Dabbelt - Engineer, SiFive

Nathaniel Graff - Software Engineer, SiFive

Networking Break

3:00pm - 3:30pm
Open RISC-V Platforms

Networking Break

3:00pm - 3:30pm
RISC-V Accelerators

Networking Break

3:00pm - 3:30pm
Secure RISC-V

Introducing New 64GC IP in the SCRx Family of the RISC-V Compatible Cores by Syntacore

3:30pm - 3:50pm
RISC-V Accelerators: Track 2

Location: 2nd Floor Meeting Room 203/204

We announce new 64bit IP in the SCRx family of the RISC-V compatible processor cores by Syntacore, including our second, high-performance 64bit Linux-capable design with SMP support. As always, newly introduced Syntacore IP are state-of-the-art clean slate designs in System Verilog, fully compatible with traditional EDA flows. In the session, we detail cores features, performance and collateral availability.

Participants

Alexander Redkin - Director, Syntacore

RISC-V Vector Performance Analysis

3:30pm - 3:50pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

We have implemented the RISC-V Vector Spec 0.5 in Spike for functional simulation, and completed an FPGA-optimized implementation for timing-accurate execution. Using several microkernel benchmarks suitable for embedded applications, individually optimized for each architecture, we evaluate the performance of the RISC-V Vector system compared to ARM NEON fixed-width SIMD instructions as well as VectorBlox variable-length vector extensions that have been optimized for use with the RISC-V base ISA. In addition to comparing performance, we investigate the individual architectural features and their area overhead so that we gain insight into the costs as well as the reasons why one architecture performs better. Current status: we have 3 benchmarks written, a Spike implementation, and a partial FPGA implementation of RISC-V vectors, and complete implementation of VectorBlox vector and NEON SIMD instructions. By the time of the summit, we expect to have ~10 benchmarks and a full FPGA implementation, as well as being up-to-date with the latest RISC-V vector spec available at that time.

Participants

Guy Lemieux - CEO, VectorBlox Computing Inc.

Keystone: An Open-Source Secure Enclave for RISC-V Processors

3:30pm - 3:50pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

Hardware enclaves reduce the trusted computing base (TCB) by excluding complex system software, while also offering integrity, confidentiality, and remote attestation for isolated user-level processes. We present Keystone, an open-source hardware enclave implementation based on the RISC-V ISA. Keystone extends from the MIT Sanctum design and removes the requirement for non-standard hardware extensions by using standard RISC-V primitives including Physical Memory Protection (PMP). Keystone can be bootstrapped on an existing RISC-V core implementing the priv-1.10 specification, provided the uncore meets a few rudimentary criteria. We will demonstrate Keystone ported to a HiFive Unleashed board. While this work focuses specifically on memory isolation with trusted DRAM, Keystone can be easily adapted for a variety of threat models including untrusted DRAM or microarchitectural side-channel attacks. Importantly, Keystone is fully open-source, and thus a compelling building block for secure system design.

Participants

Dayeol Lee - Graduate Student, UC Berkeley

Ara: 64-bit RISC-V Vector Implementation in 22nm FDSOI

3:55pm - 4:25pm
RISC-V Accelerators: Track 2

Location: 2nd Floor Meeting Room 203/204

In this talk, we detail our experience in the design and implementation of the RISC-V Vector Extensions (v0.4 draft) in an advanced silicon process. Ara is a high-performance vector co-processor soft core that attaches to and cooperates with an existing open-source RISC-V core Ariane, implementing RV64. Ara receives instructions from Ariane, which splits the instruction stream into scalar and vector parts. The vector processor instance that we implemented in silicon features four lanes, with floating-point units, a 64 KiB register file with dynamic vector length and count, independent load/store units, and has hardware to accelerate common vector reductions, such as vector summation and inner product. Two variants of the Ariane+Ara duo are combined with memory into a system-on-chip, aiming at exploring both the high-performance and low-power ends of the silicon implementation spectrum. We discuss design implementation insights, lessons learned, and tradeoffs; and we present area, performance, and power results in Globalfoundries' 22FDX FDSOI process.

Participants

Fabian Schuiki - PhD Student, ETH Zurich

Matheus Cavalcante - PhD Student, ETH Zurich

Design and Implementation of a RISC-V ISA-based In-order Dual Issue Superscalar Processor

3:55pm - 4:15pm
RISC-V Accelerators

Location: 1st Floor, Exhibit Hall A-1

This session details the microarchitecture design of an 11-stage pipelined RISC-V ISA based 64-bit processor, VAJRA64. The microarchitecture of fetch, decode and execute stages are detailed. RISC-V is a new instruction set architecture (ISA) that was originally designed to support computer architecture research and education developed by University of California, Berkeley and has been open sourced as BSD license.

Participants

Libin TT - Principal Engineer, C-DAC

S. Krishnakumar Rao - Associate Director, C-DAC

Establishing a Security Verification Framework For The RISC-V Architecture

3:55pm - 4:25pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

Today, there is a preponderance of popularity and support toward using open-source instruction set architectures such as RISC-V and their respective hardware designs due to their customizability and the ability to collaborate on successful designs. Along with these benefits, open-source hardware designs have the unique opportunity to have their microarchitectural features enhanced in a variety way of ways to improve performance. However, recent microarchitectural security exploits (such as Spectre and its variants) demonstrate that microarchitectural performance features have a dramatic impact on system security. The open-source nature of RISC-V presents an opportunity to add microarchitectural features in a secure manner without compromising performance by leveraging a Secure Development Lifecycle (SDL). In order to create a successful SDL for open-source hardware designs, several challenges need to be addressed.

In this talk, we discuss the state of hardware security in general, then discuss the unique security opportunities and challenges in open-source hardware design. Also, we will present a framework and set of techniques and methodologies for understanding the security ramifications of any microarchitectural/ architectural change that is applied to a design. Lastly, we will present an example security analysis on a real world hardware design using these techniques.

Participants

Jason Oberg - CEO, Tortuga Logic

Secure Bootstrapping of Trusted Software in RISC-V

4:30pm - 5:00pm
Secure RISC-V

Location: 2nd Floor Meeting Room 209/210

A growing concern with the diverse RISC-V ecosystem is the proliferation of security primitives which do not straightforwardly compose into secure systems. We must address this issue by creating reusable, well-understood fundamental primitives for security. One often overlooked aspect of a secure system is the process by which its trusted environment is initialized.

In this session, we discuss a secure boot procedure for a generic RISC-V processor system, one which endows a software environment with a cryptographic key pair for remote attestation, and a certificate with a cryptographic measurement of the boot image. This protocol can be used to measure and sign arbitrary software, is agnostic of hart implementation and ISA features, is appropriate for a multi-hart system (provided inter-hart interrupts are available), and executes entirely in M-mode (does not rely on hardware-assisted privilege). We rely on standard software cryptographic primitives throughout the secure boot process, namely SHA-3 hashes, ed25519 elliptic key cryptography, and an AES-256 cipher. After boot, the software system is trusted to maintain confidentiality of its secret keys, although a malicious boot image does not compromise the keys of an honest one. We discuss several mechanisms for deriving trusted device keys (commitment to a nonce, non-volatile memory, physical unclonable function), and outline how this secure boot process is used in the Sanctum and Keystone secure processors. We also discuss a work-saving technique to improve boot latency by caching encrypted keys in untrusted memory. A C and machine code implementation of this secure boot protocol is provided as open-source software, unencumbered by licenses or patents. We also demonstrate an instance of this secure boot protocol in the context of the Sanctum processor.

Participants

Ilia Lebedev - Graduate Student, Massachusetts Institute of Technology

SCHEDULE

CONFERENCE DAY 2, DECEMBER 5, 2018 - 05/12/2018

TIME	EXPO	KEYNOTES	OPEN RISC-V PLATFORMS	RISC-V ACCELERATORS	RISC-V ACCELERATORS: TRACK 2	SECURE RISC-V
8:00AM		**8:00am** - Registration Open: 8:00 AM - 5:30 PM **8:25am** - Welcome **8:30am** - A New Golden Age for Computer Architecture: History, Challenges, and Opportunities				
9:00AM		**9:00am** - Opportunities and Challenges of Building Silicon in the Cloud **9:20am** - Deepening the RISC-V Ecosystem to Drive Industry-Wide Adoption **9:40am** - Accelerating Innovation: Why Google's TPU Was Just the Start				
10:00AM	**10:00am** - Exhibit Hall Open: 10AM - 3:30PM **10:15am** - RISC-V Linux Hackathon: 10AM - 3:00PM	**10:00am** - Networking Break on the Expo Floor **10:40am** - Keynote Panel: Opportunities and Challenges in Security for Open Source Hardware				
11:00AM		**11:20am** - RISC-V: Opportunities and challenges in SoCs **11:40am** - Lunch				
12:00PM						

SCHEDULE

CONFERENCE DAY 2, DECEMBER 5, 2018 - 05/12/2018

TIME	EXPO	KEYNOTES	OPEN RISC-V PLATFORMS	RISC-V ACCELERATORS	RISC-V ACCELERATORS: TRACK 2	SECURE RISC-V
1:00PM	**1:10pm** - Exhibit Hall Open: 10AM - 3:30PM **1:30pm** - RISC-V Linux Hacakthon: 10AM - 3:00PM		**1:10pm** - Running Other Architecture Operating Systems and Applications on RISC-V Using QEMU **1:40pm** - How to Address RISC-V Compliance in the Era of OPEN ISA and Custom Instructions	**1:10pm** - Domain-Specific Acceleration via AndeStar V5 Processors **1:40pm** - The Esperanto ET-Maxion High Performance Out-of-Order RISC-V Processor		**1:10pm** - If We Get RISC-V Security Right, It Will Become the Dominant Processor in the $470B IoT Market **1:40pm** - Never Again: Spectre-Proofing Chip Designs with End-to-End Formal Methods
2:00PM			**2:10pm** - Accelerating Inferencing on the Edge with RISC-V **2:40pm** - Command-Driven Data Transfer Protocols in RISC-V SoCs	**2:10pm** - Methodologies Behind the World's First RISC-V-based SSD Controller **2:40pm** - Machine-Readable Specifications of RISC-V ISA		**2:10pm** - How to Protect RISC-V Against Side-Channel Attacks? **2:40pm** - SiFive TERP: A Trusted Execution Reference Platform for Embedded Secure Applications
3:00PM			**3:00pm** - Networking Break	**3:00pm** - Networking Break **3:30pm** - RISC-V Vector Performance Analysis **3:55pm** - Design and Implementation of a RISC-V ISA-based In-order Dual Issue Superscalar Processor	**3:30pm** - Introducing New 64GC IP in the SCRx Family of the RISC-V Compatible Cores by Syntacore **3:55pm** - Ara: 64-bit RISC-V Vector Implementation in 22nm FDSOI	**3:00pm** - Networking Break **3:30pm** - Keystone: An Open-Source Secure Enclave for RISC-V Processors **3:55pm** - Establishing a Security Verification Framework For The RISC-V Architecture
4:00PM						**4:30pm** - Secure Bootstrapping of Trusted Software in RISC-V

SESSIONS

MEMBER MEETINGS: MUST BE A RISC-V FOUNDATION MEMBER TO ATTEND - 06/12/2018

Registration & Networking

8:00am - 8:30am

Board of Directors -- CLOSED SESSION

8:30am - 10:30am
Room 212

Lunch Room and Members Lounge

8:30am - 12:30pm
Room 209/210

P Extension

9:30am - 10:30am
Room 201

Processor Trace

9:30am - 10:30am
Room 203/204

Memory Model 2.0

9:30am - 10:30am
Room 207

ISA Formal Specification

10:30am - 11:30am
Room 201

J Extension

10:30am - 11:30am
Room 203/204

Bitmanip

10:30am - 11:30am
Room 207

Marketing Events

10:30am - 11:30am
Room 212

Vector Extensions

11:30am - 12:30pm
Room 201

Marketing Content

11:30am - 12:30pm
Room 203/204

TEE

11:30am - 12:30pm
Room 207

Compliance

11:30am - 12:30pm
Room 212

Lunch

12:30pm - 1:30pm

Location: Room 209/210

Cryptographic

1:30pm - 2:30pm
Room 201

Marketing Outreach / Research

1:30pm - 2:30pm
Room 203/204

Base Ratification

1:30pm - 2:30pm
Room 207

Software

1:30pm - 2:30pm
Room 212

Lunch Room and Members Lounge

1:30pm - 3:30pm
Room 209/210

Technical Committee Chair & Vice Chair -- CLOSED SESSION

2:30pm - 3:30pm
Room 201

Marketing Committee

2:30pm - 3:30pm
Room 203/204

SSC & RISC-V SSITH

2:30pm - 3:30pm
Room 207

Fast Interupt

2:30pm - 3:30pm
Room 212

All Members Closing Session

3:30pm - 4:30pm
Room 203/204

SCHEDULE

MEMBER MEETINGS: MUST BE A RISC-V FOUNDATION MEMBER TO ATTEND - 06/12/2018

RISC-V Summit

December 3 - 6, 2018
Santa Clara Convention Center
Santa Clara, CA

TIME	ROOM 201	ROOM 203/204	ROOM 207	ROOM 209/210	ROOM 212
8:00AM	**8:00am** - Registration & Networking	**8:00am** - Registration & Networking	**8:00am** - Registration & Networking	**8:00am** - Registration & Networking **8:30am** - Lunch Room and Members Lounge	**8:00am** - Registration & Networking **8:30am** - Board of Directors -- CLOSED SESSION
9:00AM	**9:30am** - P Extension	**9:30am** - Processor Trace	**9:30am** - Memory Model 2.0		
10:00AM	**10:30am** - ISA Formal Specification	**10:30am** - J Extension	**10:30am** - Bitmanip		**10:30am** - Marketing Events
11:00AM	**11:30am** - Vector Extensions	**11:30am** - Marketing Content	**11:30am** - TEE		**11:30am** - Compliance
12:00PM	**12:30pm** - Lunch	**12:30pm** - Lunch	**12:30pm** - Lunch	**12:30pm** - Lunch	**12:30pm** - Lunch
1:00PM	**1:30pm** - Cryptographic	**1:30pm** - Marketing Outreach / Research	**1:30pm** - Base Ratification	**1:30pm** - Lunch Room and Members Lounge	**1:30pm** - Software
2:00PM	**2:30pm** - Technical Committee Chair & Vice Chair -- CLOSED SESSION	**2:30pm** - Marketing Committee	**2:30pm** - SSC & RISC-V SSITH		**2:30pm** - Fast Interupt
3:00PM		**3:30pm** - All Members Closing Session			